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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/535,233	03/24/2000	Masaya Kadono	SEL 171	1670

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)	
09/535,233	KADONO ET AL.	
Examiner	**Art Unit**	
W. David Coleman	2823	

Offic Action Summary

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicants arguments filed December 11, 2002 in paper no. 18 are not persuasive. Applicants contend that Lin et al., U.S. Patent 6,123,865 herein known as Lin fails to teach a semiconductor film formed on a semiconductor wafer.

In response to Applicants argument that Lin fails to teach a semiconductor film formed on a semiconductor wafer, Applicants are directed to column 2, lines 36-41 where Lin teaches the layer formed over the wafer being etched can be a nonmetal layer formed of silicon. It is well known in the art that silicon is recognized as a semiconductor material.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case Muraoka discloses the manufacture of a semiconductor device (column 1, line 13) and in particularly a gate oxide film (column 4, line 51).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., U.S. Patent 6,123,865 in view of Muraoka et al., U.S. Patent 4,339,340.

3. Pertaining to claims 11 and 15, Lin discloses a semiconductor process as claimed. See **FIG. 1** where Lin teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film formed over a substrate **10**;

spinning the substrate (column 1, lines 40-41);

contact an etching solution to a surface of said semiconductor film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface (etch products are removed, column 1, line 40). However, Lin fails to teach forming a gate insulating film after performing a spin etch of the semiconductor film of which the contaminating impurity has been removed. Muraoka teaches the removal of contaminants deposited on the surface of intermediate semiconductor products (see Abstract, second sentence). In view of Muraoka, it would have been obvious to one of ordinary skill in the art to incorporate the intermediate steps of Muraoka into the Lin semiconductor process because the treatment of a silicon wafer with an oxidizing acid results in the formation of a very thin oxide film on the surface of the wafer.

4. Pertaining to claims 14 and 16, Lin teaches wherein the contaminating impurity is removed by an acidic solution containing fluorine (hydrofluoric acid, column 2, lines 34).

5. Claims 13, 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., U.S. Patent 6,123,865 in view of Muraoka et al., U.S. Patent 4,339,340 as applied to claims 11 and 14 above, and further in view of Araujo et al., U.S. Patent 5,578,103.

6. The combined teachings discloses a semiconductor process substantially as claimed as discussed above. However, Lin in view of Muraoka fails to teach wherein the contaminating impurity element is at least selected from periodic table group I or periodic table group II consisting of Na, K, Mg, Ca and Ba. Araujo teaches wherein the contaminating impurity element is selected from periodic table group I. See column 2 of Araujo where sodium (Na) is taught as a contaminating impurity element from periodic table group I. In view of Araujo, it would have been obvious to one of ordinary skill in the art to incorporate the claimed contamination into the combined teaching process because sodium is a contaminating impurity from periodic table group I because sodium ions at the glass surface exchanged for hydrogen ions contaminate the liquid crystal (column 1, lines 34-35).

7. Claims 19, 20, 23, 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., U.S. Patent 6,123,865 in view of Muraoka et al., U.S. Patent 4,339,340 and Yoshikawa et al., U.S. Patent 6,106,907.

8. Pertaining to claims 19, 23 and 27, Lin discloses a semiconductor process substantially as claimed. See **FIG. 1** where Lin teaches a method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film formed over a substrate **10**;

spinning the substrate (column 1, lines 40-41);

contact an etching solution to a surface of said semiconductor film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface (etch products are removed, column 1, line 40). Please note that polysilicon is a crystallized semiconductor film. However, Lin fails to teach forming a gate insulating film after performing a spin etch of the semiconductor film of which the contaminating impurity has been removed. Muraoka teaches the removal of contaminants deposited on the surface of intermediate semiconductor products (see Abstract, second sentence). In view of Muraoka, it would have been obvious to one of ordinary skill in the art to incorporate the intermediate steps of Muraoka into the Lin semiconductor process because the treatment of a silicon wafer with an oxidizing acid results in the formation of a very thin oxide film on the surface of the wafer. Please note that gate electrodes are inherent in the formation of an electrode (usually called "gate electrode") are one of the fundamental parts of a MOS system as disclosed by Muraoka (column 1, line 53). Yoshikawa teaches that the electrode layer can be the gate wiring layer. See FIG. 7, where Yoshikawa discloses a wiring layer 3a,5a,6a and 7a. In view of Yoshikawa, it would have been obvious to one of ordinary skill in the art to incorporate the gate wiring layers of Yoshikawa into the combined teachings of Lin and Muraoka because a liquid crystal device with metal electrodes can be formed with good adhesion (see Abstract of Yoshikawa, last sentence).

9. Pertaining to claims to claims 20, 24 and 28, Lin teaches wherein the contaminating impurity is removed by an acidic solution containing fluorine (hydrofluoric acid, column 2, lines 34).

10. Claims 21, 22, 25, 26, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., U.S. Patent 6,123,865 in view of Muraoka et al., U.S. Patent

4,339,340 and Yoshikawa et al., U.S. Patent 6,106,907 as applied to claims 19, 20, 23, 24, 27 and 28 above, and further in view of Araujo et al., U.S. Patent 5,578,103.

11. The combined teachings discloses a semiconductor process substantially as claimed as discussed above. However, Lin in view of Muraoka fails to teach wherein the contaminating impurity element is at least selected from periodic table group I or periodic table group II consisting of Na, K, Mg, Ca and Ba. Araujo teaches wherein the contaminating impurity element is selected from periodic table group I. See column 2 of Araujo where sodium (Na) is taught as a contaminating impurity element from periodic table group I. In view of Araujo, it would have been obvious to one of ordinary skill in the art to incorporate the claimed contamination into the combined teaching process because sodium is a contaminating impurity from periodic table group I because sodium ions at the glass surface exchanged for hydrogen ions contaminate the liquid crystal (column 1, lines 34-35).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

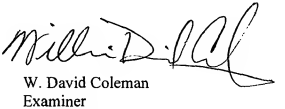
13. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



W. David Coleman
Examiner
Art Unit 2823

WDC
March 5, 2003